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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/665,558	09/22/2003	Tatsuo Nishino	XA-9930	6170

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EXAMINER	
CASIANO, ANGEL L	
ART UNIT	**PAPER NUMBER**
2182	

DATE MAILED: 03/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/665,558	NISHINO ET AL.	
	Examiner	Art Unit	
	Angel L. Casiano	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/22/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

- The present Office action is in response to application filed 22 September 2003.
- Claims 1-21 are pending.

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on 9/22/2003 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

3. Claims 5, 7, 8, 11, and 15 are objected to because of the following informalities:

a. Claim 5 (Page 4, line 1), "transfer" and "device" are missing letters.

b. Claim 7 (Page 4), "interface" is missing a letter

c. Claim 7 (Page 5, line 1), "parallel" is missing a letter

d. Claim 8 (Page 5), "the" is missing letter *e*

e. Claim 8 (page 6), "the" is missing letter *e*

f. Claim 11 (Page 7, line 1), "controller" is missing letter *e*

g. Claim 15 (Page 8), "predetermined" is missing letter *e*

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 15-19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

6. Claim 15 recites the limitation "an address designating unit which can designate the address of transfer buffer" in the data processor. However, the claim does not refer to a *transfer buffer* previous to this limitation.

In addition, claim 15 (see line 4) recites, "execute **the** data transfer for **the** external device". The claim does not make reference to "data transfer" or "external device" earlier in the language.

7. There is insufficient antecedent basis for these limitations in the claim. Claims 16-19 depend directly or indirectly upon claim 15 and are therefore rejected under the same basis.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1-3, 5-8 and 15-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Butler et al. [US 6,260,086 B1].

Regarding claim 1, Butler et al. teaches a data processor having a semiconductor chip (see Figures 1 and 2, "100"; col. 2,

lines 43-44) including a central processing unit (see "CPU 125", col. 2, line 40); an interface controller (see "210", "215", "220", and "230") to perform input and output of data to and from an external side of the semiconductor chip; and a bus controller (see "225" and "235") connected with an external bus (see Figure 1, and col. 2, line 60), wherein said interface controller includes an interface control unit (see col. 8, lines 32-37, "215"), FIFO unit (see col. 8, lines 30-31; see also "220" and "230"), and a transfer control unit (see col. 8, lines 24-29 and "205"), wherein said interface control unit (see "215") outputs data from the FIFO to an external side of the semiconductor chip and inputs the data inputted from the external side of the semiconductor chip to the FIFO unit (see col. 8, lines 35-37, *control logic 210, 215 output data to EEPROM via shift register "225" and "235"*), and wherein the transfer control performs the control transfer data stored the FIFO unit by designating a transfer destination address and the control to input the data to the FIFO unit by designating a transfer source address (see col. 8, lines 25-29 and col. 5, lines 15-20).

As for claims 2 and 3, Butler et al. teaches a transfer control unit inputting data and designating destination address

in parallel to the read of data (from a source address) (see "*data is transferred in parallel*", col. 2, lines 58-62).

Regarding claim 5, Butler et al. teaches a data processor having a semiconductor chip (see Figure 1, "100"; col. 2, lines 43-44 and col. 8, lines 56-58, "*embodied in a single integrated circuit*") including a central processing unit (see "CPU 125", col. 2, line 40); an interface controller for inputting and outputting data to and from an external side of the semiconductor chip; and a bus controller connected to an external bus (see Figure 1, and col. 2, line 60), wherein said interface controller includes an interface control unit (see col. 8, lines 32-37), FIFO unit (see col. 8, lines 30-31), and a general purpose transfer control device (see col. 8, lines 24-29), wherein said interface control unit outputs the data from the FIFO to an external side of the semiconductor chip and inputs data inputted from the external side said semiconductor chip said FIFO unit (see col. 8, lines 35-37), and wherein said transfer control performs the control transfer data stored the FIFO unit by designating a transfer destination address and the control to input the data to the FIFO unit by designating a transfer source address (see col. 8, lines 25-29).

As for claims 6 and 7, Butler et al. teaches a transfer control unit inputting data and designating destination address in parallel to the read of data (from a source address) (see "*data is transferred in parallel*", col. 2, lines 58-62).

Regarding claim 8, Butler et al. teaches a data processor having a semiconductor chip (see Figure 1, "100"; col. 2, lines 43-44) including a central processing unit (see "CPU 125", col. 2, line 40); an interface controller to perform input and output of data to and from an external side of the semiconductor chip; and a bus controller connected with an external bus (see Figure 1, and col. 2, line 60), wherein said interface controller includes an interface control unit (see col. 8, lines 32-37), and a transfer control unit (see col. 8, lines 24-29), wherein said interface control unit outputs data from a FIFO to an external side of the semiconductor chip and inputs the data inputted from the external side of the semiconductor chip to the FIFO unit (see col. 8, lines 35-37), and wherein the transfer control performs the control transfer data stored the FIFO unit by designating a transfer destination address and the control to input the data to the FIFO unit by designating a transfer source address (see col. 8, lines 25-29).

The reference also teaches a RAM (see Figure 2, "Ram 316") as well as data transfer (*inputting data and outputting data to and from a predetermined region of the RAM*, see col. 2, lines 1-3).

Regarding claim 15, Butler et al. teaches a data processor having a semiconductor chip (see Figure 1, "100"; col. 2, lines 43-44) including a central processing unit (see "CPU 125", col. 2, line 40); an interface controller to perform input and output of data to and from an external side of the semiconductor chip; and a bus controller connected with an external bus (see Figure 1, and col. 2, line 60), wherein said interface controller includes an interface control unit (see col. 8, lines 32-37), transfer buffer (see *FIFO*, col. 8, lines 30-31), and a general purpose transfer control unit (see col. 8, lines 24-29), wherein said interface control unit outputs data from the FIFO to an external side of the semiconductor chip and inputs the data inputted from the external side of the semiconductor chip to the FIFO unit (see col. 8, lines 35-37), and wherein the transfer control performs the control transfer data stored the FIFO unit by designating a transfer destination address and the control to input the data to the FIFO unit by designating a transfer source address (see col. 8, lines 25-29).

As for claim 16, Butler et al. teaches providing the transfer buffer in the control unit (see Figure 1, "220" and "230").

As for claim 17, Butler et al. teaches a RAM (see Figure 2, "Ram 316").

As for claim 18, Butler et al. teaches the RAM for data transfer (*inputting data and outputting data to and from a predetermined region of the RAM*, see col. 2, lines 1-3).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for

establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

12. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

13. Claims 4, 11-14 and 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Butler et al. [US 6,260,086 B1] in view of Luke et al. [US 6,959,350 B1].

As for claims 4 and 20-21, Butler et al. does not teach the interface controller as being a USB interface controller. Luke

et al. explicitly teaches a USB interface controller (see Figure 1, "12"). At the time of the invention, one of ordinary skill in the art would have been motivated to combine the cited disclosures in order to implement the apparatus in combination with USB device, such as "facsimile (Fax), copier, and printer" wherein the "interface controller includes configuration circuitry generated from a configuration package" as taught by Luke et al. (see col. 1, lines 40-45 and col. 2, lines 30-34).

Regarding claim 11, Butler et al. teaches a data processor over a semiconductor substrate (see Figure 1, "100"; col. 2, lines 43-44) including a CPU (see "125", col. 2, line 40); an interface controller to perform input and output of data to and from an external side of the semiconductor chip; and a bus controller connected with an external bus (see Figure 1, and col. 2, line 60), wherein said interface controller includes a FIFO buffer (see col. 8, lines 30-31), and a data transfer control device (see col. 8, lines 24-29).

Butler et al. does not teach the interface controller as being a USB interface controller. In addition, the Butler et al. reference does not teach a DMA controller. Luke et al. explicitly teaches a USB interface controller (see Figure 1, "12") and a DMA controller (see col. 2, lines 26-27). At the

time of the invention, one of ordinary skill in the art would have been motivated to combine the cited disclosures in order to implement the apparatus in combination with USB device, such as "facsimile (Fax), copier, and printer" wherein the "interface controller includes configuration circuitry generated from a configuration package" as taught by Luke et al. (see col. 1, lines 40-45 and col. 2, lines 30-34).

As for claim 12, Butler et al. teaches an interface control device that designates a transfer destination address and a transfer source address (see col. 8, lines 25-29).

Regarding claim 13, Butler et al. teaches a data processor over a semiconductor substrate (see Figure 1, "100"; col. 2, lines 43-44) including a CPU (see "125", col. 2, line 40); an interface controller to perform input and output of data to and from an external side of the semiconductor chip; and a bus controller connected with an external bus (see Figure 1, and col. 2, line 60), wherein said interface controller includes a FIFO buffer (see col. 8, lines 30-31), and a data transfer control device (see col. 8, lines 24-29). Butler et al. also teaches a RAM (see Figure 2, "RAM 316").

Butler et al. does not teach the interface controller as being a USB interface controller. In addition, the Butler et al. reference does not teach a DMA controller. Luke et al. explicitly teaches a USB interface controller (see Figure 1, "12") and a DMA controller (see col. 2, lines 26-27). At the time of the invention, one of ordinary skill in the art would have been motivated to combine the cited disclosures for the reasons stated above.

As for claim 14, Butler et al. teaches a RAM (see Figure 2, "Ram 316") as well as data transfer (*inputting data and outputting data to and from a predetermined region of the RAM*, see col. 2, lines 1-3).

14. Claims 9-10 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Butler et al. [US 6,260,086 B1] in view of Eisele [US 2002/0109869 A1].

As for claim 9, Butler et al. teaches accessing via the external bus through the bus controller (see Figure 1) but it does not teach generating address for making access in FIFO format to the predetermined region of the RAM. Eisele teaches reading data from the RAM via a FIFO memory (see Page 7,

paragraph [0033]). At the time of the invention, one of ordinary skill in the art would have been motivated to combine the cited disclosures in order to obtain an apparatus for processing raster data in a printer, as taught by Eisele (see Page 1, paragraph [0002]).

As for claim 10, Butler et al. does not teach read and write operations performed in halves of a transfer cycle. Eisele teaches a controller generating read/write cycles in order to read data from a source (see Page 3, paragraph [0033]). At the time of the invention, one of ordinary skill in the art would have been motivated to combine the cited disclosures for the reasons stated above.

As for claim 19, Butler et al. does not teach the data processor in which read and write operations are performed in halves of a transfer cycle. Eisele teaches a controller generating read/write cycles in order to read data from a source (see Page 3, paragraph [0033]). At the time of the invention, one of ordinary skill in the art would have been motivated to combine the cited disclosures for the reasons stated above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Angel L. Casiano whose telephone number is 571-272-4142. The examiner can normally be reached on 9:00-5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on 571-272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alc
01 March 2006

KIM HUYNH
SUPERVISORY PATENT EXAMINER
3/8/06